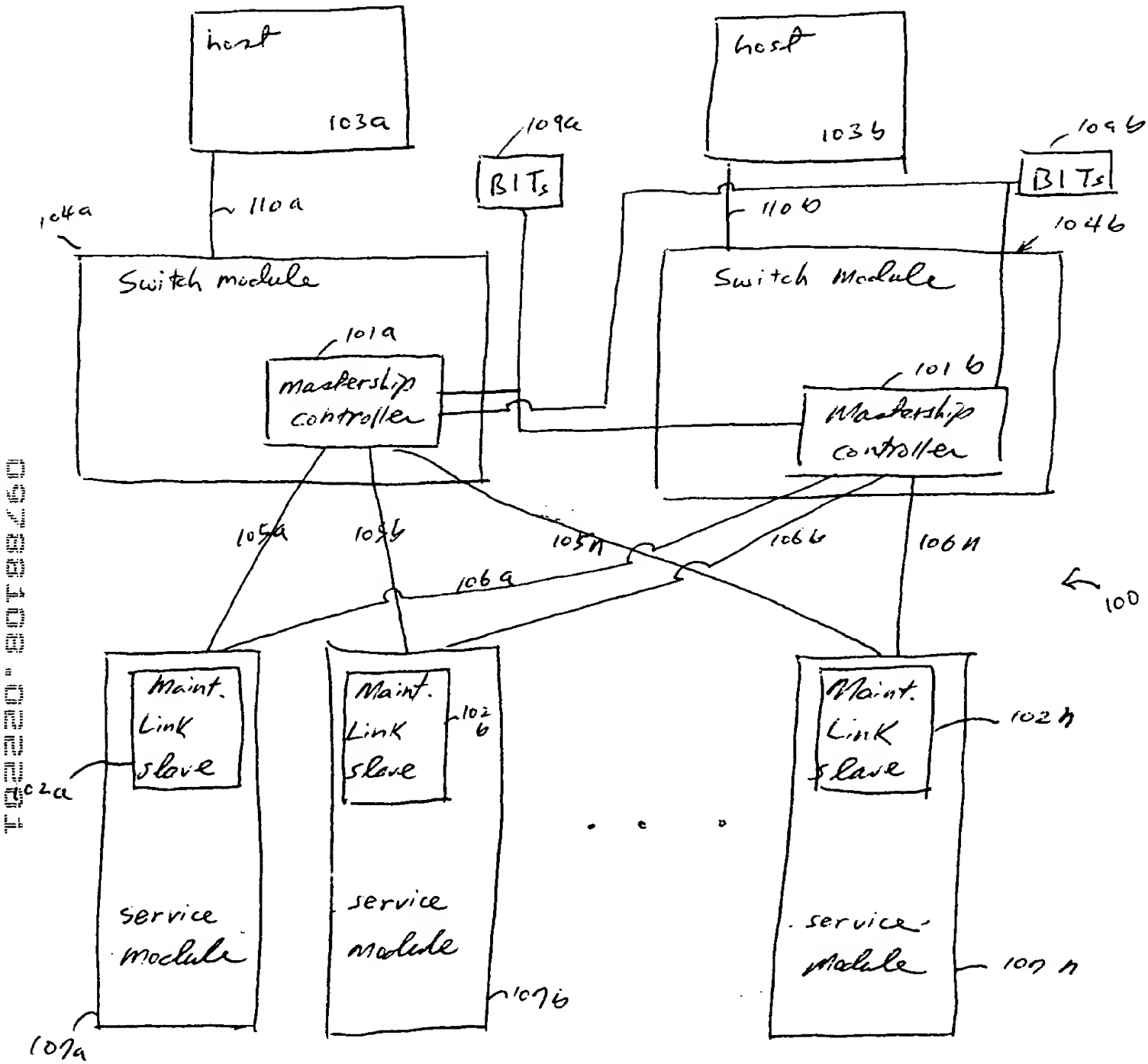
host
103a
host
103b
109a
BITs
109b
BITs
110a
110b
104a
104b
Switch module
Switch Module
101a
mastership controller
101b
mastership controller
105a
105b
105n
106a
106b
106n
100
Maint. Link slave
102a
Maint. Link slave
102b
Maint. Link slave
102n
service module
107a
service module
107b
service module
107n

Figure 1

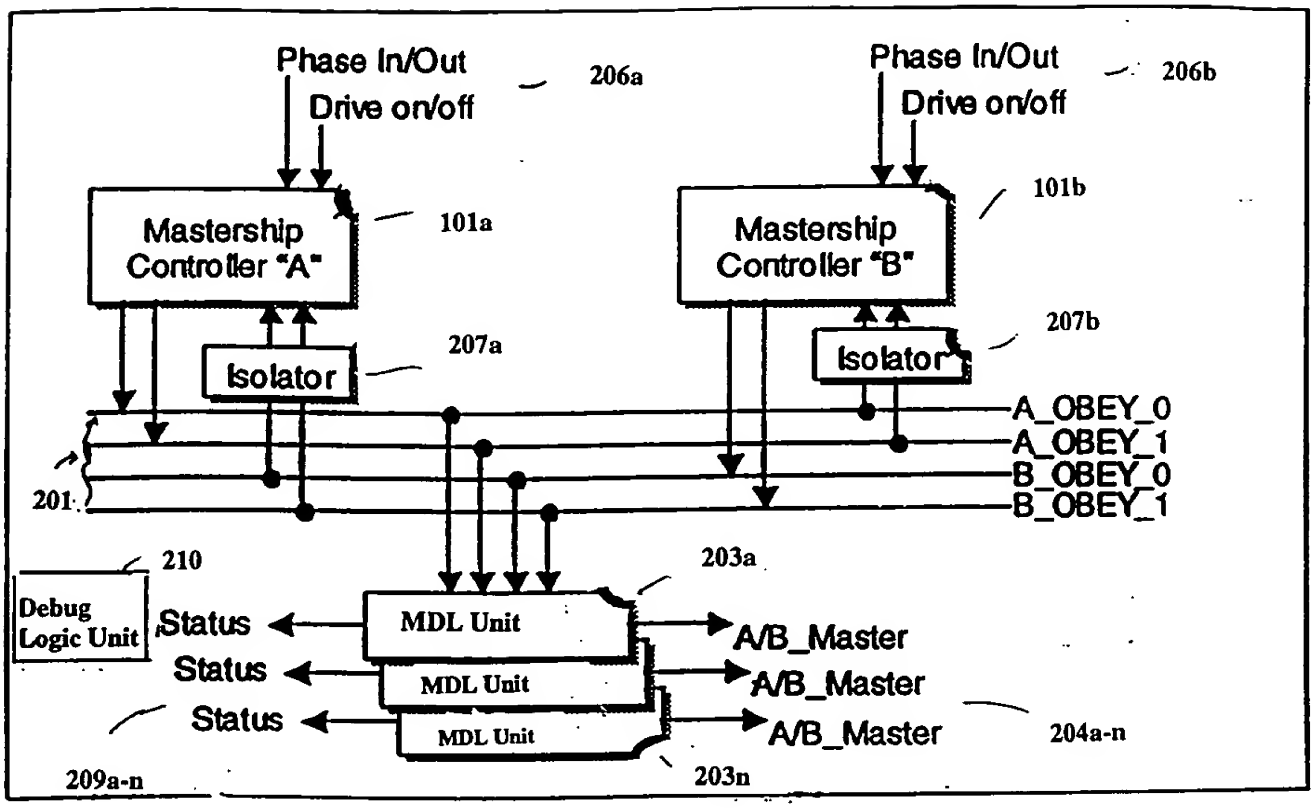

Figure 2: Mastership circuitry

A-OBEY	B-OBEY	Phase	Controller to be Working	Comments
None	None	N/A	A	Abnormal condition, included for completeness: normally one controller should want to be master
Clocking	None	N/A	A	Controller_B absent, faulted, or doesn't want to be master
None	Clocking	N/A	B	As above, but for Controller_A
Clocking	Clocking	IN	A	Both controllers are functioning correctly, and A is as the master controller
Clocking	Clocking	OUT	B	Both controllers are functioning correctly, and B is as the master controller

Figure 3: Mastership rules with clocked mastership lines